

S. Stevenson  
#2  
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09/820468  
03/28/01

EL465781655US

Inventor: Werner Juengling, et al.

Title: Methods of Forming Materials Between Conductive Electrical Components and Insulating Materials

Assignee: Micron Technology, Inc.

Priority Serial No. 09/115,339

Priority Filing Date: July 14, 1998

**INFORMATION DISCLOSURE STATEMENT**  
**PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98**

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional application of co-pending application Serial No. 09/115,339, filed July 14, 1998. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2).

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: March 28, 2001

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Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-1599	PRIORITY SERIAL NO. 09/115,339		
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Werner Juengling et al.			
				PRIORITY FILING DATE July 14, 1998	PRIORITY GROUP 2813		
U.S. PATENT DOCUMENTS							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	3,919,060	11/11/75	Pogge et al.			
	AB	3,979,230	9/7/76	Anthony et al.			
	AC	3,998,662	12/21/76	Anthony et al.			
	AD	4,063,901	12/20/77	Shiba			
	AE	4,180,416	12/25/79	Brock			
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	AJ	5,583,078	12/10/96	Osenbach			
	AK	5,599,745	2/4/97	Reinberg			
FOREIGN PATENT DOCUMENTS							
	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
	AL						
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AR		HOMMA, TETSUYA, "Low Dielectric Constant Materials and Methods for Interlayer Dielectric Films in Ultralarge-Scale Integrated Circuit				
			Multilevel Interconnections", <u>Materials Science &amp; Engineering</u> , R23, pp. 243-285 (1998)				
	AS		ABSTRACT: Townsend, P.H., et al., "SILK Polymer Coating With Low Dielectric Constant and High Thermal Stability for ULSI Interlayer				
			Dielectric", <u>The Dow Chemical Company</u> , Midland, MI, 9 Pages, (Undated)				
	AT		PRODUCT BROCHURE and MATERIAL SAFETY DATA SHEET, "Interlayer Dielectric", <u>JSR Microelectronics</u> , 12 Pages (1997)				
EXAMINER				DATE CONSIDERED			
<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>							

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-1599		PRIORITY SERIAL NO. 09/115,339	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Werner Juengling et al.			
				PRIORITY FILING DATE July 14, 1998		PRIORITY GROUP 2813	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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	AE	5,773,363	6/30/98D	erderian et al.			
	AF	3,954,523	05/76	Magdo et. al.	148	175	
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	AT		Watanabe, H., "A Novel Stacked Capacitor with Porous-Si Electrodes for High Density DRAMs", Microelectronics Research Laboratories, NEC Corp., date unknown, pp. 17-18.				
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	AM	6,001,747	12/1999	Annappagada			
	AN	S/N 09/948,372		Leonard Forbes et al.			10/9/97
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		Document Number	Date	Country	Class	Subclass	Translation
							Yes      No
	AO						
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AQ		Peter Singer (Editor-in-Chief); "The New Low-k Candidate: It's a Gas"; Technology News, March 1989, 1 page				
	AR		ABSTRACT: Anderson, R.C. et al., "Porous Polycrystalline Silicon: A New Material For MEMS", Jnl. Of Microelectromechanical Systems (Mar. 1994), Vol. 3, No. 1, pp. 10-18				
	AS		Stanley Wolf, "Silicon Processing for the VLSI Era", Vol. 1, Sunset Beach, CA; Lattice Press, pp. 429-437.				
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